SPECIFICATION

Electronic Version 1.2.8

Stylesheet Version 1.0

REFRESHING OF MULTI-PORT MEMORY IN INTEGRATED CIRCUITS

Background of Invention

[0001] Integrated circuits, such as digital signal processors (DSPs), use on-chip memory (memory module) to store information to be processed. The on-chip memory comprises, for example, an array of static random access memory cells or alternatively dynamic random access memory cells. The memory cells are connected to wordlines travelling in one direction and to bitlines travelling in another direction. Dynamic memory cells comprise a storage capacitor and at least one access transistor. The charge stored in the storage capacitor is indicative of the information stored (e.g., logic 0 or logic 1). Due to leakage effects the charge in the storage capacitor dissipates over time. The stored charge, therefore, has to be refreshed periodically to ensure that the memory cell maintains the correct information during the operation of the IC.

[0002] In some applications, a dual port memory module, is used. A dual port memory module includes first and second ports through which the memory cells can be accessed. Each port includes signal lines for receiving address, data and control signals. Each port, for example, includes an address decoder which selects a particular wordline or row of memory cells within the memory cell array. The memory cells are connected to both access ports by two separate wordlines and two separate bitlines.

[0003] The memory cells of the array must be refreshed after a specified time (e.g., retention time). However, the refresh cycle may coincide with the occurrence of an access request to the memory cell array through either one of the access ports. Conventionally, accesses to the memory module are halted until the refresh cycle is

completed, which adversely impacts performance of the system.

[0004] From the foregoing discussion, there is a desire to provide a multi-port memory module in which the adverse impact on system performance by the refresh cycle is reduced.

Summary of Invention

[0005] The invention relates generally to ICs with a memory module. In particular, the invention relates to efficiently refreshing a multi-port memory module. In one embodiment, the memory modules include first and second ports. A control block manages the memory accesses and refresh requests. In one embodiment, the control block includes a contention detection circuit that monitors the memory access requests through the access ports as well as the refresh operations. A refresh counter provides the sequence of addresses of rows of memory cells that are to be refreshed. The addresses of memory accesses rows are provided through the access ports. The address decoder within each port activates the row either for a refresh or for a memory access. The contention circuit ensures that a refresh operation is allocated to a port which is not used for a memory access at the same time.

Brief Description of Drawings

[0006] Fig. 1 shows a block diagram of a dual port memory;

[0007] Fig. 2 shows a particular memory cell of the memory cell array shown in Figure 1;

[0008] Fig. 3 shows a diagram of a refresh cycle;

[0009] Fig. 4 shows a functional diagram of a refresh control circuit; and

[0010] Fig. 5 shows an alternative timing diagram of a refresh cycle.

Detailed Description

[0011] Fig. 1 shows a block diagram of a dual-port memory module in accordance with one embodiment of the invention. The memory module, for example, could be embedded into an IC, such as a DSP. Other types of ICs, such as memory ICs, are also useful. As shown in Fig. 1, the memory module includes a memory array 1 which can be accessed through first and second ports 2 and 3 (port A and port B). Providing a

memory module with additional memory arrays or additional ports is also useful. The memory module, for example, can be accessed by multiple signal processors or micro-controllers.

[0012] The memory array 1 comprises a plurality of memory cells 11 arranged in a rows 13 and columns 14. A row of memory cells includes first and second wordlines 103a-b. The first wordlines are controlled by a first row decoder 21a and the second wordlines are controlled by a second row decoder 21b. A column of memory cells includes first and second bitlines 101a-b. First sense amplifiers 107a are coupled to first bitlines and second sense amplifiers 107b are coupled to second bitlines.

[0013] Fig. 2 shows a dual-port memory cell in accordance with one embodiment of the invention. The memory cell comprises two access transistors 110, 111 and a storage transistor 112, which drain and source terminals are connected to the transistors 110, 111. The gate electrode of the storage transistor 112 is biased by the upper supply potential V_{DD}, when n-channel-MOS-transistors are used. Alternatively, p-channel-MOS-transistors can be used. In this cases, the gate electrode of the storage transistor is biased by the lower supply potential V_{SS}. The drain/source path of transistor 110 is connected to a first bitline 101, the drain/source path of transistor 111 is connected to a second bitline 102. The gate electrodes of transistors 110, 111 are connected to separate wordlines 103 and 104, respectively. Bitline 101 and wordline 103 are connected to port A; wordline 104 and bitline 102 are connected to port B. In alternative embodiment, other types of dual port or multi-port memory cells can be used in the memory module. To access the memory cell through either of the ports, the respective wordline is activated and is brought to a high potential (V_{DD}) to make the respective access transistor conducting. Activating the wordlines with a boosted voltage which is greater than V_{DD} is also useful.

[0014]

Referring back to Fig. 1, a control block 4 is provided to control accesses to the memory array. The control block, for example, is a state machine. Other types of circuit or logic block can also be used. The control block receives control signals, such as read/write and address information and in response generates signals for accessing the memory module. To access the memory module through port A, the control block generates active CSA signal and the address of the memory cell to be

accessed (ADRA). An RWA signal is also generated. Depending on whether the access is a read or write access, the RWA signal will either be a logic 1 or logic 0. For example, RWA is equal to a logic 1 for a read access and a logic 0 for a write access. Similarly, if the access is through port B, CSB and address of the memory cell (ADRB) are generated along with RWB to indicate whether the access is a read or write. Data is provided during a write access or retrieved during a read access (e.g., DATAA, DATAB).

[0015] In accordance with one embodiment of the invention, the control block includes a refresh control block for controlling the refresh operations. Providing a refresh control block which is separate from the control block is also useful. In one embodiment, the refresh control enables memory accesses to the memory module during a refresh operation.

[0016] The refresh control block generates refresh enable (RE), refresh row address (RR), and wait (WSB) signals and outputs them to the respective control inputs of the ports A and B. These signals will later be to be explained. The control circuit 4 comprises multiplexers 41-46 that output alternative signals for the normal access to a port and for a refresh access.

[0017] Fig. 3 shows the refresh timing in accordance with one embodiment of the invention. The refresh is performed within a refresh cycle 50 between the time instances 0 and T. Two refresh cycles 50a-b are separated by the refresh idle time I. The retention time R is the combination of refresh cycle time T and idle time I. The retention time R is selected such that the charge stored within the storage capacitors is sufficiently high enough to be correctly detected for a subsequent refresh. During a refresh cycle 50 all n rows of the memory cell array have to be refreshed. In one embodiment, the n rows are refreshed sequentially through either the first or second port. The memory cells are refreshed by, for example, performing a read access to the memory cells of a row. The refresh operation is repeated n times for all n rows of the cell array. After the expiration of the retention time R, the same procedure is repeated.

[0018] Fig. 4 shows an operational diagram of a control circuit 4 in accordance with one embodiment of the invention. The control circuit, for example, is a state machine. The

control circuit comprises a control block 61. The control block receives a system clock signal which controls the function of the memory module. The IC can have two modes of operation, poser down or normal. The operating modes of the IC can be controlled by the PD signal. In one embodiment, a second clock signal is provided to the control block. The second clock signal is generated by, for example, an oscillator 60.

[0019] In one embodiment, the control generates a refresh enable signal (RE). The refresh control signal can be synchronized with either of the clock signals. The RE signal controls a refresh address counter 62 that provides the sequence of the row addresses of the memory cell array. The refresh address counter outputs the refresh address RR. In one embodiment, if the IC is in power down mode (e.g., PD = 1), the refresh is activated using the refresh clock from oscillator 60 by function block 63. In the power down mode, the IC is not susceptible to access requests through ports A and B.

[0020] When the IC is in normal operation (e.g., PD = 0), the refresh address RR is forwarded to function block 64 which performs contention detection. Contention detection is performed, in one embodiment, by comparing the address of the access and refresh address. Function block 64 is provided with any addresses ADRA, ADRB subject to an access through port A or B and the port select signals CSA, CSB. During a refresh operation, four different contention scenarios or states can occur, as shown in Table 1.

[0021]

[t1]

Table 1

State	Port A	Port B	Refresh allocation
1	–	–	Port A/Port B
2	√	–	Port B
3	–	√	Port A
4	√	√	Port B

State 1 represents the case where no memory access is requested during a refresh

request. In the absence of a contention between a refresh and a memory access, the row addressed by the refresh counter can be refreshed through either of the ports. In a preferred embodiment, one of the ports can be dedicated for refreshing (e.g., port A) when no contention occurs.

[0022] State 2 represents the case where a memory access is requested through port B while a refresh is requested. The addresses of the refresh and access are compared. If the addresses of the access and refresh are to different rows, the access is conducted through port B while the refresh operation is allocated to port A. The row corresponding to the refresh address is refreshed through port A. Alternatively, a memory access through port B is requested simultaneously with a refresh request, as represented by state 3. In such a case, the memory access is performed through port B while the refresh is conducted through port A if the addresses of the access and refresh are to different rows.

[0023] In one embodiment, for states 2 or 3, where an access is a read access to the same row which is to be refreshed, the refresh is suppressed or omitted. All the memory cells of the row are read. However, only data from the selected cell or cells of the row is output. The reading of the cells effectively refreshes the row. For a write operation, the non selected cells of the row are read without outputting their data. Alternatively, the refresh can be performed from on port while the access is performed from the other port.

[0024] In the case where memory accesses via both ports are requested along with a refresh request (state 4), one of the accesses is performed through one of the ports while a refresh is performed through the other port if neither of the accesses is to the row which is to be refreshed. The second access is delayed with a wait signal until the refresh is completed. The wait signal also informs that the access to other port is delayed. For example, the access to port A is performed, the access to port B is delayed, and the refresh is performed through port B. Assigning priority to port B for memory accesses in such a case is also useful. The priority of access to the ports can be rotated through the use of a flag.

[0025] In the case where one of the accesses is to a row which is to be refreshed, the refresh operation can be disabled. Both rows can be accessed. In the case where a

write access is performed to a memory cell on the row which is to be refreshed, the selected memory cell is written to while the other memory cells of the row are read.

[0026] When port A or port B is used for the refresh, the row decoder in the respective port A or B is provided with the address of the row from the refresh address counter.

[0027] The function block 64 performing the function of contention detection and address comparison performs the following decisions:

[0028] 1. When RE = 0, then there is no conflict between port access and refresh. The row address ADRA is provided to the first decoder through its input ADRA', the row address ADRB is provided to the second decoder through its input ADRB'. Decoders activate one of the wordlines to read or write data from or into one or several of the memory cells of a row.

[0029] 2. When RE = 1 and none of the ports A or B is selected for an external access, the refresh address RR is provided to one of ports A and B through one of their inputs ADRA' and ADRB'.

[0030] 3. When RE = 1 and only port A is selected for an external access, the row address ADRA for the access through port A is provided to first row decoder. The refresh address RR is provided to second row decoder to perform the refresh.

[0031] 4. When RE = 1 and only port B is selected for an external access, the row address ADRB for the access through port B is provided to the second row decoder. The refresh address RR is provided to first row decoder for refresh.

[0032] 5. When RE = 1 and both ports A and B are selected for an external access, the address ADRA for access of port A is provided to first row decoder to perform the requested access. The refresh address RR from refresh address counter 62 is provided to second row decoder to perform the refresh. In addition, a wait cycle signal WSB is issued by refresh control block 4 to delay the read/write address with respect to row address ADRB by one cycle so that the refresh cycle can be performed through the second row address decoder of port B.

[0033] In all of the cases 3 through 5 it is assumed that the refresh address RR from refresh address counter 62 is different from the read/write addresses ADRA, ADRB. If

this is not the case and the refresh address RR is equal to one of the row addresses ADRA, ADRB which are intended for an access, the refresh of the particular row is suppressed. Also in case 5 the issuance of the wait cycle signal WSB is omitted. Instead, the access is performed. The function block 64 contains a comparator that compares the row addresses of memory cells to be accessed for read/write and the row address for a refresh.

[0034] In Fig. 5 an alternative time scheme is shown to perform the periodic refresh of the memory cell array. The time period between the pulses 71 and 72 of the refresh enable signal RE is the same as in Fig. 3. The refresh enable signal, however, has a sequence of shorter pulses as compared to Fig. 3 and is repeated several times. The refresh enable signal is distributed over the period R over N pulses. Whereas all N rows are refreshed in time period 0, T according to Fig. 3, only one of the N rows is refreshed in one of the pulses (e.g., 71 in Fig. 5).

[0035] While the invention has been particularly shown and described with reference to various embodiments, it will be recognized by those skilled in the art that modifications and changes may be made to the present invention without departing from the spirit and scope thereof. The scope of the invention should therefore be determined not with reference to the above description but with reference to the appended claims along with their full scope of equivalents.